Electronic properties of metal/sol-gel SiO_2/indium-phosphode capacitor

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This work reports on the electrical properties of metal-oxide-semiconductor (MOS) capacitors made with a spin-on-glass (SOG) SiO_2 layer, doped with 2% phosphorus, deposited on InP substrate by spin casting followed by a low-temperature (<260 °C) anneal. The capacitance versus voltage behavior as well as the dielectric constant of the SOG layer was analyzed as a function of the frequency. The stability of the relevant parameters was checked after a long period of time (four weeks), compared with fresh devices, and revealed a significant increase in the dielectric constant and a slight increase in the leakage current. It is shown that the use of SOG as the dielectric material in the MOS structure leads to a relatively low fixed charge (less than 2×10^{11} cm^{-2}) and low fast state concentration.

Indium-phosphide (InP) metal-insulator-semiconductor field-effect transistor (MISFETs) have important potential applications in high-frequency digital circuits, microwave power amplifiers, and monolithic optoelectronics circuits. High electron mobility (5200 cm/V s) and high saturation velocity (2.5×10^7 cm/s) are the two key properties which make InP attractive for this application. The InP MISFETs can be readily configured for enhancement-mode operation, thus allowing low-power dissipation to be achieved in digital circuits. As a result of the insulated gate, a large dynamic range for the circuit can be achieved leading to a larger logic swing and consequently better noise margins. The larger breakdown voltage, higher thermal conductivity, and lower ionization coefficient compared to GaAs make InP a better choice for microwave power generation. The semi-insulating nature of InP makes circuit isolation easy and minimizes cross talk. InP is expected to play an important role in optical fiber telecommunications since the long-wavelength optical devices use InP as the substrate. The band-gap energy of InP-based alloys is near the wavelength of minimum loss in optical fibers.

For example, monolithic integration of an InGaAs photodetector and an electronic signal processing circuit using InP MISFETs on the same chip is possible for optical communication applications. Compared to GaAs, InP is far more suitable for MISFET applications because the density of interface states near the conduction-band edge is small enough[1] provided that appropriate insulator formation condition is employed. Since InP decomposes at temperatures larger than 350 °C dielectric deposition at lower temperature is mandated. Early efforts were directed at the development of an InP MIS technology using anodic[2,3] and thermal[4,5] oxides as gate insulators. However, the use of such oxides was abandoned due to the low resistivity ($r\approx10^{12}$ Ω cm) and large density of interface states near the midenergy gap ($1\text{–}5\times10^{11}$ cm^{-2} eV^{-1}). To date, the best results for an InP MIS structure have been achieved with deposited dielectric layers such as: SiO_2 using direct and indirect chemical vapor deposition (CVD)[6–8] pyrolytic[9,10] and photo-CVD[11,12] techniques. These techniques have provided SiO_2 with resistivity higher than 10^{15} Ω cm, dielectric constant of 3.9–4.0, index of refraction of 1.46–1.48, and breakdown field strengths higher than 5×10^6 V/cm. The reported density of states of InP capacitors with CVD oxide is 2×10^{11} cm^{-2} eV^{-1} (Ref. 6), and 5×10^{11} cm^{-2} eV^{-1} (Ref. 7) while Refs. 9 and 10 report on a density of states of $1\text{–}2\times10^{11}$ cm^{-2} eV^{-1} for pyrolitic CVD oxide.

The most serious problem for InP MISFETs in practical exploitation is the drain current instability owing to the slow trapping and detrapping of channel electrons by the interface traps. Van Vechten and Wager[13] proposed that surface defects such as phosphorous vacancies account for the hysteresis in the capacitance-voltage (C-V) characteristics and the drain current drift in the MISFETs. These modes seem to be realistic since surface defects are generated during gate dielectric deposition.[14] Encouraging results in minimizing the drain current drift in InP MISFETs achieved in the last few years by using low-temperature processes and different techniques of phosphorus surface saturation during the initial step of the gate deposition. Pande and Gutierrez[15] reduced drift by saturating the InP surface with phosphorus vapor and subsequently forming a $P_2O_xN_{1-x}$ layer with a SiO_2 gate dielectric. Mikami *et al.*[16] suppressed the current drift using $P_2O_xN_{1-y}$ gate insulator. Meiners[6] used phosphorus-doped Al_2O_3. Schachter *et al.*[17] used 500–2000 A of amorphous phosphorus layer in the InP MIS structure, and achieved low density of states (10^{11} cm^{-2} eV^{-1}) near the conduction-band minimum. These results indicate that the saturation of the InP surface, with either arsenic or phosphorous, reduces the surface defect density.

In the present work a phosphorus-contained spin-on-

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glass (SOG) SiO_2 layer is used as the dielectric gate film. The results presented in this letter include electrical characterizations of the MOS structures such as capacitance-voltage (C-V) analysis, leakage currents, breakdown voltage, and dielectric constants. The possible use of such layers is demonstrated as an alternative for P saturated dielectric deposition method which can be obtained in a very simple, easy, cost effective way and at low temperature.

The InP substrates were of ⟨100⟩ crystal orientation and effective carrier concentration of 3×10^{15} cm^{-3}. After a standard cleaning procedure the semiconductor surface was analyzed by Auger electron spectroscopy to control the composition, homogeneity, and the absence of organic residuals. Silicon substrates, ⟨100⟩, phosphorus doped (5×10^{14}–10^{15} cm^{-3}) were also used as substrates for comparison.

Phosphorus-doped (2%) SOG-type OCD-2P made by Tokyo-Ohka, Inc. was used. The material was deposited by spin casting and was dryed at 125, 180, and 260 °C for 90, 90, and 30 s, respectively. Undoped SOG-type 110 made by Allied Signal Inc. was used for reference and was processed the same as the doped SOG.

Another SOG, the Allied Signale Inc. siloxane material type Allied 110, was tested on the silicon reference wafers. This is an undoped material which contains a significant amount of carbon when processed at temperatures up to 260 °C. Following the SOG deposition, aluminum dots (1.2 μm thick, 500 μm diameter) were evaporated on the heated samples (150 °C) through a shadow mask. To assure good back contacts, a thin Au-Ge/Ni/Au (1000/200/1000 A) layer was evaporated on the back side of the wafer and the sample was heated to 330 °C for 3 min in vacuum. The capacitors were measured in the 10 Hz–10 MHz range using the HP 4274 multifrequency capacitance meter. The I-V characteristics of the capacitors were measured with the HP 4145B semiconductor parameter analyzer.

Typical capacitance versus voltage of the SOG/InP MOS capacitor are presented in Fig. 1. We present data for the frequency range 200 Hz–100 kHz; data for higher frequencies up to 2 MHz were almost identical in shape to the curve at 100 kHz. The data presented in Fig. 1 are for a fresh device, i.e., stored in a dry nitrogen ambient and measured within two weeks of its making. The capacitance flatband voltage was calculated assuming an n-type doping level of about 3×10^{15} cm^{-3}. The high-frequency C-V curves exhibit hysteresis and the slope at the depletion region depends on the scan direction. The C-V curves scanned from inversion to accumulation are steeper than those of the reverse scan. This indicates a less density of states near midgap while scanning from inverse to accumulation compared to the reverse scan. The flatband voltage of the C-V curve scanned from inversion to accumulation, $V_{FB}^{I\rightarrow A}=-1.2\pm0.05$ V, depends on the fixed charge Q_F and the metal-semiconductor potential, ϕ_{ms}. The flatband voltage of the C-V curve scanned from accumulation to inversion $V_{FB}^{A\rightarrow I}=-0.95\pm0.05$ V, depends also on Q_F and ϕ_{ms} but also on the charge trapped near the

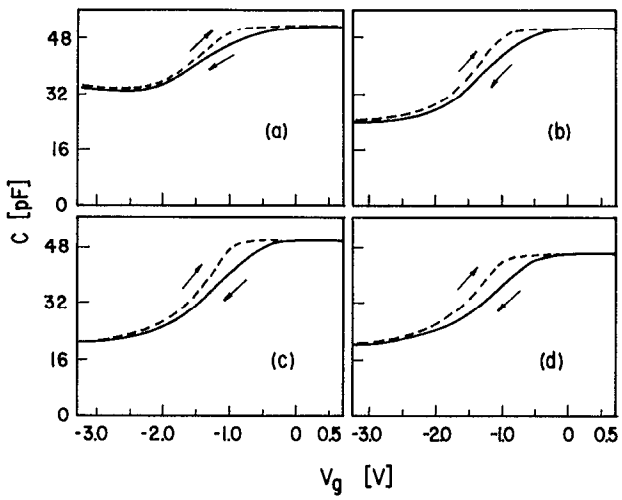

FIG. 1. High-frequency C-V curves of SOG MOS capacitor on InP measured at (a) 200 Hz, (b) 1 kHz, (c) 10 kHz, and (d) 100 kHz.

interface, Q_{it}. Since $\Delta V_{FB}=V_{FB}^{A\rightarrow I}-V_{FB}^{I\rightarrow A}\simeq0.25$ V, we estimate $Q_{it}\simeq-3\times10^{10}$ cm^{-2}. ΔV_{FB} depends on the scan span; it is about 50 mV for sweeps between $+1$ to -1 V and 250~300 mV for sweeps between $+1$ to -3 V. The calculated fixed charge concentration depends on the value of ϕ_{ms}. Taking the work function of aluminum, the affinity, and the doping of the InP one can find that Q_F is on the order of 2×10^{11} cm^{-2}. The minimum capacitance at negative bias was found to increase as the frequency decreases. This may be due to minority-carrier generation in the inversion layers.

The capacitance was found also to vary with the frequency. Typical accumulation-capacitance versus frequency is plotted in Fig. 2. Curve (a) of Fig. 2 describes the accumulation-capacitance for a fresh device. After four weeks exposure to air the device capacitance increased dramatically and the device accumulation-capacitance versus frequency is presented in curve (b) of Fig. 2. After annealing in vacuum at 250 °C for 30 min the accumulation-

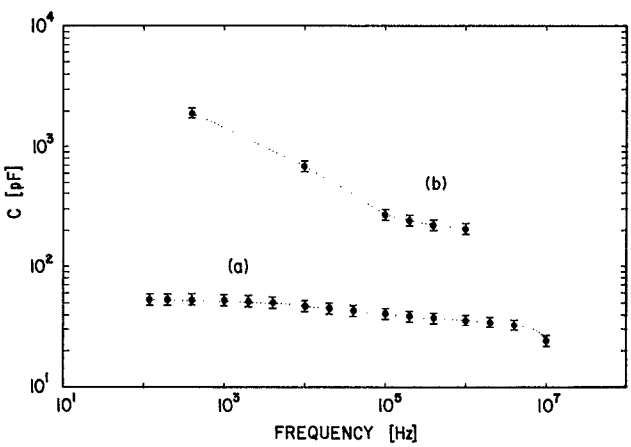

FIG. 2. Accumulation oxide capacitance of silicate SOG (2% phosphorus) MOS InP capacitor as a function of frequency is shown: (a) as is (immediately after preparation) and (b) after one month.

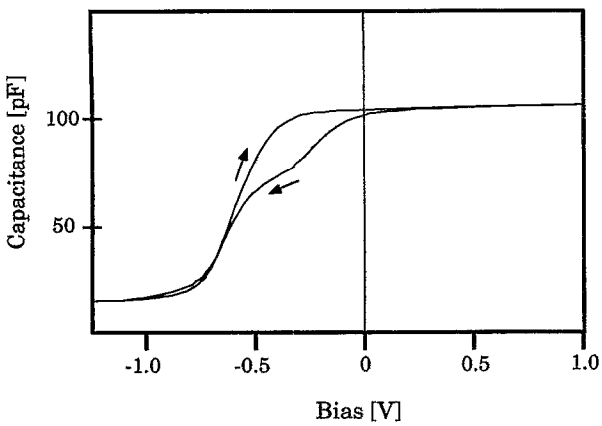

FIG. 3. High-frequency (100 kHz) *C-V* curves of silicate (2% phosphorus) SOG MOS capacitor on silicon. The device was measured from accumulation to inversion and back.

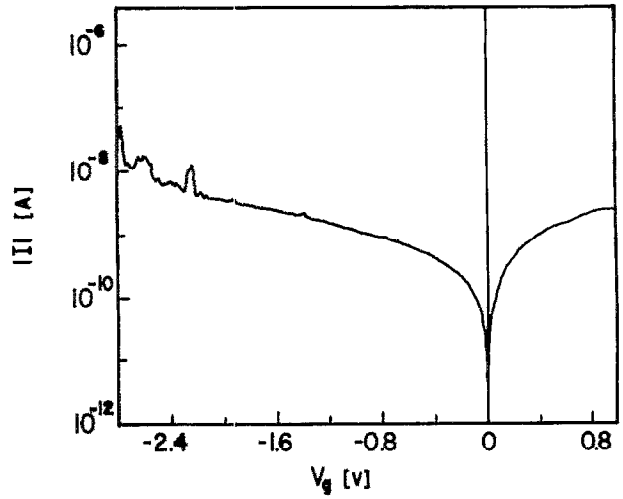

FIG. 4. Typical *I-V* curve of MOS capacitor with silicate SOG (2% phosphorus) dielectric layer on InP substrate.

capacitance decreased and became the same as that of a fresh device. The capacitance increase after exposure to air was not accompanied by any significant change in the surface and bulk parameters, or an increase of the device leakage current. It could be explained by assuming a large increase of the SOG dielectric constant. The extracted ϵ_{ox} of fresh P-doped silicate SOG on InP is about 3.9–4.0. at low frequencies. It decreases only slightly as a function of the frequency up to 1 MHz. After exposure to air ϵ_{ox} increases by a factor of 4 at 100 kHz and by a factor of 40 at 1 kHz. Between 1–100 kHz it decreases as w^{-p}, where w is the frequency and $p = 0.3$–0.5, and its decrease becomes more moderate above 100 kHz.

The reference silicon MOS devices were analyzed and a typical *C-V* curve of a device with P-doped silicate SOG is shown in Fig. 3. Sweeping from inversion to accumulation sol-gel capacitors had a fixed surface charge density of less than 10^{11} cm^{-2}, and low midgap density of states ($< 10^{11}$ cm^{-2} eV^{-1}). The reverse sweep, from accumulation to inversion, indicated the formation of a large localized trap level near the conduction band. This trap level was not observed in the undoped siloxane SOG (Allied 110) devices. The siloxane devices *C-V* curves showed little hysteresis and were very similar to those of the doped silicate capacitors as measured from inversion to accumulation. Sol-gel films made on silicon showed a different dielectric constant and stress than that of the same materials prepared on indium phosphide and gallium arsenide. It is believed that the sol-gel films structure, and therefore their physical and electrical properties, depend on the substrate thermal expansion and contraction during the spin casting and the annealing process. Therefore, the properties of metal/SOG/semiconductor devices depend not only on the effect of the insulator on the substrate but also on the substrate effects on the insulator.

Typical *I-V* characteristics of such device are presented in Fig. 4. The device leakage current which reflects the quality of the layer as an insulating material was found to be rather high and exceeds 10^{-6} A/cm^2 at 1 V (specific resistivity of about 5×10^{13} Ω cm at 1 MV/cm). For larger bias the current increases and instabilities were observed at about 2×10^{-6} A/cm. A typical breakdown field of such oxide, as determined by *I-V* ramp, is in the range of 1–2 MV/cm.

To summarize, phosphorus-doped SOG has been demonstrated for low-temperature passivation of InP. This SOG may be sensitive to moisture but a vacuum anneal at 250 °C can restore the MOS device characteristics to their original values.

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